# Design and Implementation of a Deep Space Communications Complex Downlink Array

**Melissa Soriano, Stephen Rogstad, Robert Navarro, Douglas Wang**
**Jet Propulsion Laboratory, California Institute of Technology**
**4800 Oak Grove Dr.**
**Pasadena, CA 91109**
**818-393-7632**
**Melissa.A.Soriano@jpl.nasa.gov**

*Abstract*— **This paper describes the design and implementation of a frequency domain beamformer that will downlink array the signals of up to eight 34-m or 70-m antennas at each of NASA's three Deep Space Communications Complexes (DSCC). The array digitizes inputs with an Intermediate Frequency (IF) of 100 to 600 MHz, coherently combines the inputs digitally, and transforms the combined waveform back to analog. Real-time correlation measurements are used for delay and phase calibration, allowing the system to adjust for atmospheric variations. A DSCC Downlink Array system is operational at each DSCC. Initial results from passes with the New Horizons spacecraft are presented and system performance is analyzed.**

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## 1. INTRODUCTION

The Deep Space Network (DSN) is NASA's network of antennas responsible for tracking and communicating with deep space missions. The DSN has three DSCCs worldwide, located in Goldstone, California, Madrid, Spain, and Canberra, Australia. Each DSCC has one 70-m antenna, multiple 34-m antennas, and related hardware. The DSN is currently constructing additional 34-m antennas and plans to have a total of four at each DSCC.

The DSCC Downlink Array (DDA) provides the ability to array four 34-m antennas to obtain an aperture area comparable to a single 70-m antenna. Alternatively, 34-m antennas can be added to a 70-m to provide augmented aperture. The DDA digitally correlates and coherently combines up to 8 antennas or inputs at a complex using frequency domain beamforming [1]. The combined signal is the converted back into analog form. The DDA accepts inputs at an Intermediate Frequency band from 100 to 600 MHz. The output analog combined signal provides increased sensitivity that can be fed into the DSN's existing receiver hardware.

The DDA will replace the existing Full Spectrum Processor Array (FSPA), which can array four inputs with a bandwidth of up to 16 MHz. The FSPA supports operations for Voyager, Spitzer, and Kepler. The FSPA also arrayed two 34-m antennas as a back up to the 70-m for Mars Science Laboratory Entry, Descent, and Landing and one of Juno's Deep Space Maneuvers. The DDA uses similar operator directives and system interfaces as the FSPA. The DDA also leverages hardware and software development performed for the Breadboard Array (BBA) [2]. The BBA was a 3-antenna array at JPL that demonstrated a frequency domain beamformer implemented in firmware working together with software processes to calculate delays and antennas weights. These feedback algorithms have been are also implemented in the DDA [4, 5].

In this paper, we present an overview of DSCC Downlink Array, its design and implementation. A system description is provided in Section 2, followed by architecture and implementation in Sections 3 and 4, respectively. Current and planned tests are presented in Section 5 and system performance is analyzed. Finally, in Section 6 conclusions are reached.

## 2. SYSTEM DESCRIPTION

The DDA's primary users will be spacecraft that are so far away that their signals are very weak, such as Voyager, New Horizons, and Juno. These spacecraft will benefit most from the DDA's ability to combine several antennas to increase antenna sensitivity. The DDA will fit into the existing DSN infrastructure at each DSCC. The desire for compatibility with all current and future missions made it especially challenging to define requirements for the system.

### *Requirements*

The DDA is required to process high bandwidth signals from eight antennas simultaneously with at least 8-bit resolution and must coherently combine these signals in real-time. The antennas are far enough apart for the Earth's rotation to cause a Doppler frequency shift between them. The DDA must also track changing delay due to the Earth's

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rotation. In addition to these known delays, the troposphere causes random path delay fluctuations that result in phase and delay differences across the antennas. The DDA must continually compensate for all these types of delays. Telemetry bandwidths of 500 MHz down to 1 kHz must be supported, requiring a large range of channel and sub-channel bandwidths. The total combining loss must be less than or equal to the previous FSPA system.

*DSN Interfaces*

The DDA interfaces with several other DSN subsystems, including the Frequency and Timing Subsystem (FTS), Service Preparation System (SPS), Network Monitor and Control (NMC) system, and Downlink Telemetry and Tracking (DTT) subsystem. FTS provides the 1 Pulse-per-second (PPS) and 100 MHz input signals used for timing. The DDA utilizes various types of spacecraft predicts files from SPS for operation. Radiometric predicts files provide the expected downlink frequencies for the spacecraft. Geocentric predicts provide the spacecraft position in right ascension and declination, as well as other ephemeris data. Telemetry predicts provide information about the telemetry mode, such as modulation type, subcarrier frequency, and symbol rate. A site coordinates file provides the location of each antenna at the DSCC. The NMC provides real-time monitor and control of all DSN subsystems. Operators may control the system in one of two ways, with ASCII text directives or through the DDA GUI. Both interfaces ultimately send data from the NMC to the DDA. The DDA will send back event notifications to report current system status to the NMC. The DDA will also publish information to the NMC about its configuration and status, including information about each DDA IF input describing which antennas are assigned, the measured signal to noise ratio of the combined signal, and combining gain to measure array performance. The DDA will also publish various plots to the NMC (for example, time histories of measured signal to noise ratio). This information will be used to evaluate performance and trending metrics. The DDA's combined analog output will be input to the DTT receiver. The DDA's interfaces to the FTS, SPS, NMC, and DTT subsystems are shown in Figure **1**. Communications between the DDA and the SPS and NMC subsystems is via the DSCC local area network.

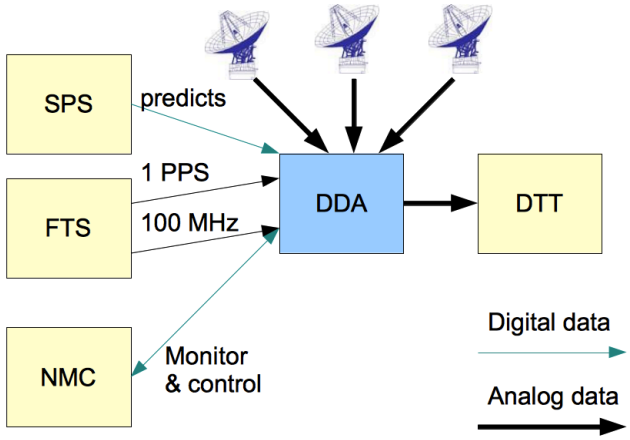


Figure 1- DDA Interfaces to other DSN subsystems

*Operations Concept*

Array operations are different from most DSN operations because multiple antennas are involved for each spacecraft pass. SPS may deliver predicts packages to the DDA via sftp at any time. Operations begins when an antenna is assigned through the NMC interface. The DDA initializes itself, performs a self-test, then parses the predicts and site coordinates files and loads configuration information into its database. The radiometric predicts files specify the spacecraft ID, RF band, and pass number. The geocentric predicts files specify the spacecraft position. A software process for modeling the input calculates the delta frequencies and delays for every centisecond using the radiometric and geocentric predicts files. The DDA begins digitizing, cross correlating and monitoring. Based on telemetry predicts and antenna assignment directives, combining is enabled or disabled as needed. The DDA operator may display input status, time history, and spectrum plots as desired. The DDA automatically weights antennas based on performance, then up-converts the combined signal to analog IF and provides it to the DTT.

*Operator Directives*

The operator may send directives to the DDA to control its operations. The DDA was designed to run as autonomously as possible. When the DDA is placed in a link connection, directives are automatically issued to setup the appropriate IF inputs. During a nominal pass, directives are automatically issued to the DDA to assign and release antennas based on the Schedule of Events. These directives specify a particular Deep Space Station (DSS) or antenna to add to the array, along with its start and stop times. Directives may also be used by the operator to override the predicts and other configuration settings if needed.

## 3. HARDWARE DESIGN AND IMPLEMENTATION

The DDA is designed to be modular and flexible. The subsystem is divided into the following major functional blocks: the beamformer, control, and feedback (BCF) unit, the Array Clock and Timing (ACT) unit, the IF to Digital (I2D) units, the Array Signal Processor (ASP) units, and the Digital to IF (D2I) unit. A DDA system diagram is shown in Figure **2**.

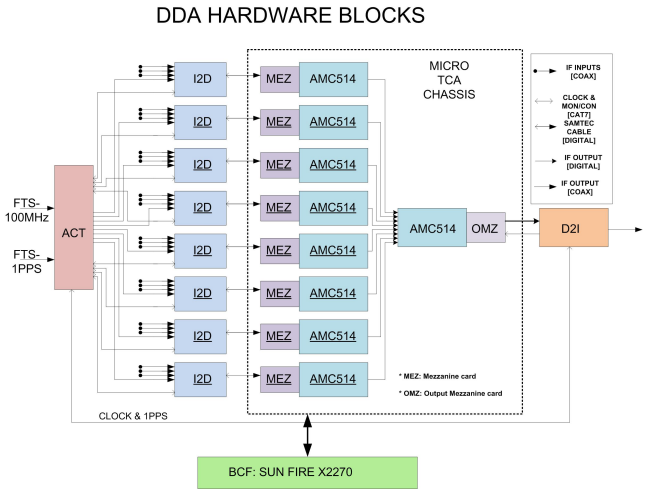


Figure 2- DDA system diagram

*Beamforming, Control, and Feedback*

The BCF unit is responsible for centralized control of the system, including parsing of the input predicts files, communications with NMC, calculation of the geometric models, and calculation of the phase and delay adjustments needed to keep the array calibrated. The BCF is a Commercial Off-the-Shelf (COTS) computer that runs Linux and JPL-developed software. More detail on the software processes is provided in Section 4.

*Array Clock and Timing*

The Array Clock and Timing (ACT) unit takes as input an 100 MHz clock reference signal and a 1 PPS time reference from FTS and generates a common 1280 MHz sampling clock and synchronized 1 PPS signal. A copy of the 1280 MHz clock and synchronized 1 PPS signal is sent to each of the eight I2Ds and the D2I. Another functionality of the ACT is to generate a common test signal for the digitizers. The test signal is a variable synthesized frequency with stable phase noise characteristics. The ACT is controlled by an embedded single board computer and is housed in a 1U rack mounted chassis. The electronics are placed on a Clock and Timing (CAT) board, which has a Clock Synthesizer (CSYN) module mounted into it. The CAT board includes a Xilinx FPGA that runs custom firmware.

*IF to Digital*

Each IF to Digital (I2D) unit processes one IF input for a total of eight inputs at a time. Each I2D unit includes a Analog to Digital converter (A2D) module with ADC chips from National Semiconductor together with IF input switching, automatic gain control and an anti-aliasing filter housed in a 1U chassis. Each I2D can select from four possible inputs using a coaxial switch. A passive anti-aliasing filter selects the 100-600 Mhz band and the IF Amplifier (IFA) provides either manual or automatic gain control. A block diagram is shown below.

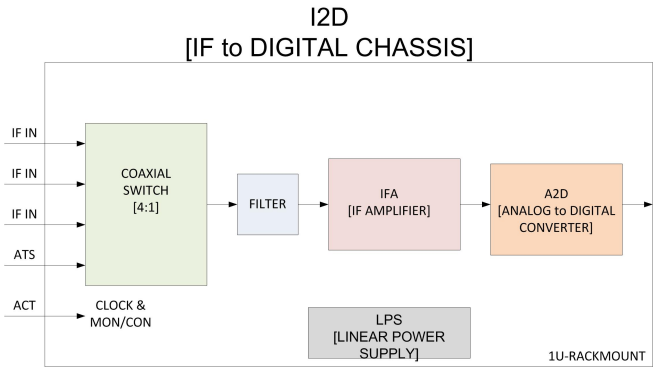


Figure 3- I2D Block Diagram

*Array Signal Processor*

Each of the eight I2D modules is associated with an Array Signal Processor (ASP) that is responsible for beamforming, including channelization, correlation, and combining (CCC). The ASP implements a frequency domain beam former with a filterbank that breaks the sampled data into 512 contiguous channels, each of 1.25 MHz bandwidth.

Telemetry with data rates that have an effective bandwidth of less than 1 MHz are not handled effectively by the 1.25 MHz channels because cross-correlations used to provide phase and delay feedback are not well matched to the signal bandwidth. This leads to less than optimal cross-correlation signal to noise ratios. The ASP can alternatively use 128 subchannels with adjustable bandwidths from 78.125 kHz down to 5 Hz to flexibly handle low rate telemetry signals for the purposes of forming cross-correlation pairs well matched to the signal bandwidth. Subchannels are a new addition that was not implemented in the FSPA or BBA. The placement of subchannels is flexible with respect to channels. Each sub-channel can be in a different channel or some may share a common channel.

The ASPs are Commercial Off-The Shelf (COTS) Vadatech AMC514 FPGA carrier cards based on the micro Telecommunication Communication Architecture (uTCA) standard. This card features a Virtex6 (XC6VLX240T) FPGA and an onboard PowerPC Processor (Freescale QorIQ P1011) with a PCIe x4 connection to the FPGA. The FPGA runs firmware that implements the heart of the digital signal processing of the DDA system. Each ASP also has two 10 Gb Ethernet ports. Communication with the BCF computer is through a 1-Gb Ethernet connection.

Communication with the FPGA on the AMC card is through a one lane PCIe bus. The 10 Gb Ethernet connections between the nine ASPs and the uTCA switch are shown in Figure **4**.

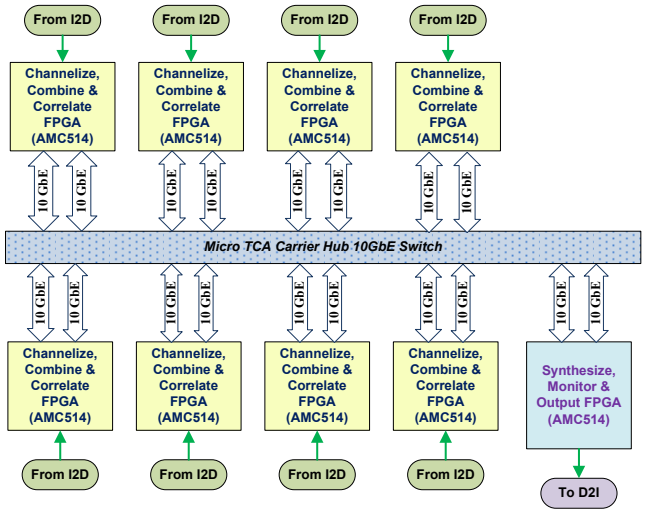


Figure 4- CCC and SMO ASPs in the uTCA Chasssis

Key challenges for the firmware included high data rates. The data is sampled at 1280 MHz and with 8-bit resolution, yielding about 10 Gbps per antenna. In the DDA, beamforming is implemented using 512 channels that are oversampled, allowing near-perfect reconstruction of the signal [1]. With oversampling, the digital data rate for each IF input is 12.8 Gbps. Since each CCC FPGA requires IF data from all 8 antennas, over 89.6 Gbps would be required to be received by each CCC FPGA. The frequency domain decomposition into 512 channels is used here to split data processing and transport among the 8 CCC FPGAs. Each CCC FPGA sends 64 channels to each of the other CCC FPGAs and receives 448 channels from the other 7 CCC FPGAs. In this way, the total data transported between FGPAs is limited to less than 20 Gbps.

The ASPs are housed in a Vadatech VT857 1U chassis with 12 Advanced Mezzanine Card (AMC) slots. The chassis contains a 26-port 10 Gb Ethernet switch and provides up to 20Gb/s connectivity from board to board. Connectivity is facilitated by using raw Ethernet packets and static, fixed, mac addressing. The uTCA chassis holds 9 AMC cards. Eight of them have beamformer functionality. The ninth synthesis, monitor, and output (SMO) ASP receives combined signals from a fraction of the input bandwidth from multiple CCC FPGAs and synthesizes those into a single time domain data stream, then formats the data to support the final A2D conversion.

The Mezzanine card on each ASP takes digitized samples from the I2D chassis and buffers them before interfacing the signals to the FPGA on the AMC514 Array Signal Processing card. The Mezzanine card uses the FPGA Mezzanine Card (FMC) form factor to allow it to be mounted on the AMC514 card, thus providing a convenient interface point for each I2D to each AMC514 card of the ASP.

Each ASP has a two 3-wire Serial Peripheral Interface (SPI) busses that are used to communicate with the I2D and CAT. The I2D SPI bus is used to monitor and control the attenuation of the IFA and control the coax switch. The IFA has a manually controlled gain mode as well as an automatic gain control (AGC) mode that sets the gain based on the input signal characteristics. The CAT SPI bus provides information such as the lock status of the 1 PPS and CSYN, 100-MHz amplitude, and CAT board temperature.

*Digital to IF*

The Digital to IF (D2I) unit accepts 1 PPS and 1280 MHz clock inputs from the ACT. It takes the digital data from the SMO ASP, formats it for conversion to analog, and then performs the digital to analog conversion using an Analog Devices AD9739.

## 4. Software Design and Implementation

The DDA is housed in a standard DSN rack. An assembled rack ready for shipping (with cables removed) is shown in *Figure* ***5***. From top to bottom, the nodules shown are uTCA chassis with the nine ASPs, the ACT, the eight I2D modules, the BCF computer.


Figure 5- DDA Assembled Rack

*Beamformer, Control, and Feedback*

The BCF software has been implemented on two types of systems: SUN FIRE X2270 M2 Server and Dell PowerEdge Server. The Sunfire servers have a quad-core processor, 12 GB of memory and a 1 TB SATA disk, with a height of 1 rack unit. The Dell PowerEdge server has an 8-core processor and 8 GB of memory. Both systems run a 64-bit Debian Linux operating system. The BCF software is a combination of shell scripts, Python scripts, and C software. The nmc_if process interfaces with the NMC, accepting connection information and publishing monitor data and plots. Another process handles support data such as predicts, determining which files to load into the database. System configuration information is stored in a PostgreSQL database that can be queried or modified by any process. The BCF also hosts all of the ASP filesystems.

The most critical BCF functionality is accomplished by the models (bcf_models) and feedback (bcf_feedback) processes. Every second, the models processes uses the predicts information about the position of the spacecraft and station positions to calculate phase and delay for each centisecond of the following second. These values are sent to each of the eight CCC ASPs, where ASP software pushed the appropriate values into FPGA registers. The ASP firmware channelizes the data into 512 channels, correlates, and combines. The correlation records from the eight CCC ASPs are read by the BCF feedback process, which calculates antennas weights that are fed back into the system [3]. Antennas that are weak or non-performing are automatically weighted down. Channel placement is controlled by the feedback process and is based on measurements and on the expected telemetry profile [4]. This flow of data between the BCF and ASP software processes is shown for a single ASP in *Figure* ***6***. A single BCF models, feedback, and read process interacts with all nine of its corresponding ASP processes.

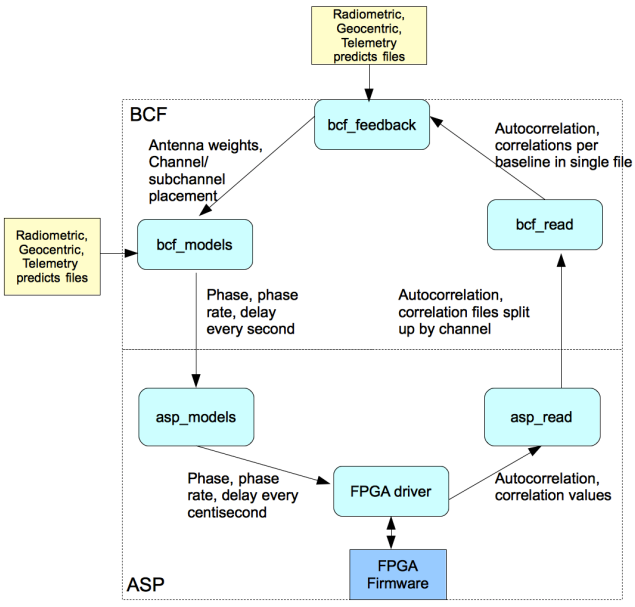


Figure 6- BCF and ASP models and feedback processes

*Array Signal Processor*

The ASP software runs on a PowerPC processor (PPC) located on each AMC514. The main purpose of the PowerPC processor and the ASP software is to provide real-time control and monitoring of the FPGA on the AMC card. The ASP operating system is Debian Linux. Most of the ASP software is written in C. A driver on ASP linux operating system exposes the memory mapped register interface of the FPGA to user space. Also, an interrupt is supported that has a period of 1 centisecond and is derived from a 1 PPS timing input that comes from FTS via the FMC on the board.

The ASP software is primarily designed to provide high level interfaces to FPGA resources, I2D resources, and ACT resources for use by the BCF. Some ASP processes are designed for use during configuration and testing. ASP software is also responsible for managing the delay frequency predicts and corelation data interfaces to the FPGA. Asp_init handles one-time initialization such as FPGA 10 GbE MAC addresses configuration, clock synchronization, ADC calibration, and sets up delays. Asp_tpg controls the Test Pattern Generator implemented in the FPGA and was used extensively during development and system testing. The test pattern generator can be configured for various carrier, subcarrier, and symbol frequencies, with variable clock delay and a noise option. Asp_flags reports system state such as clock and lock status, coax switch position, temperatures and power supply voltages, IF amplifier attenuation, and firmware versions. Asp_sample samples data streams from different points in the FPGA, including the raw ADC input so that various statistics such as amplitude and rms can be calculated. This capability is especially valuable in testing and diagnostics.

The ASPs use Network Time protocol (NTP) for keeping time to within one second, with the BCF as a reference. For subsecond timing, the ASP firmware maintains a centisecond register that is referenced to the 1 PPS signal. Several ASP commands latch and become effective on the next 1 PPS. Synchronized timing between the BCF and all ASPs is critical. Many ASP commands are designed to be schedulable for a time in the future. During initial DDA configuration, BCF system can send commands to all ASPs and schedule their execution a few seconds in the future to ensure that the commands on all ASPs occur at the same second. The ASPs use their internal clocks based on the 1 PPS signal to determine time within the second.

The two primary persistent ASP processes are asp_models and asp_read. Asp_models is responsible for obtaining a phase, phase rate, delay, and gain values from bcf_models every second and writing these values to the appropriate FPGA firmware registers every centisecond. Each Asp_read process is responsible for reading 64 channels of cross-correlation data for 28 baselines from the ASP's FPGA registers and writing them to a file, where they are

collated by bcf_read and read by the BCF feedback process. The BCF feedback process uses these correlation records for array calibration.

The BCF computer maintains a network connection to multiple ASP embedded processors. Linux shell level commands are used for operation of each AMC card running ASP software. These shell commands allow for both normal operations and debug and development efforts. Each command is autonomous and the ASP keeps no central database of its own. State information between ASP programs is kept in FPGA register memory.

The FPGA Linux Driver provides access to the firmware memory map through a process that is compiled at the kernel level (a kernel object or .ko file). This driver is intended to be simple and generic, so that all developers use a single instance. This structure, coupled with the .ko file, provides developers the ability to code directly to the memory map in a simple fashion.

## 5. TESTING

Full system testing is challenging due to the myriad of possible array scenarios. The DSN supports a broad range of carrier and subcarrier frequencies, and telemetry rates among many spacecraft. There is also a desire for the DDA to support future missions. System testing at JPL included 8-input arraying with the test pattern generator and the following signals:

- pure carrier offset by a different delay for each input + noise
- carrier + 50 MHz telemetry
- carrier + 100 kHz telemetry

The system will also be tested using several spacecraft to verify key capabilities.

Acceptance test cases include the following:

- Nominal scenario: 3 antennas, 1 comes/goes, nominal/off-nominal
- 2 antennas, dual polarization (New Horizons spacecraft)
- Low rate telemetry, low power, X-band (Voyager spacecraft)
- 2 antennas, Ka-band (Kepler spacecraft)

A DDA system will be delivered to the Goldstone DSCC in December for test passes with the New Horizon spacecraft. New Horizons nominally downlinks data using an X-band carrier with a 25 kHz subcarrier for telemetry. Expected signal-to-noise-ratio is about 31 dB-Hz.

## 6. CONCLUSIONS

A new DSCC Downlink antenna Array (DDA) for the Deep Space Network has been designed, implemented, and deployed. The DDA coherently combines up to 8 inputs at an IF band from 100 to 600 MHz using a frequency Domain Beamforming Architecture. This architecture provides flexibility to handle multiple antennas at very high data rates. The DDA supports telemetry bandwidths from 500 MHz down to 1 KHz using channels and sub-channels.

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## BIOGRAPHIES

***Melissa Soriano*** *is a senior software engineer in the Tracking Systems and Applications Section at the Jet Propulsion Laboratory. She is the DDA Software Cognizant Engineer and has been working on arraying for 10 years at JPL. She has a B.S. from Caltech, double major in Electrical and Computer Engineering and Business Economics and Management. She also has an M.S. in Computer Science from George Mason University.*

***Stephen Rogstad*** *is the group supervisor of the Processor Systems Development Group (PSDG) at JPL. He received his B.S. and M.S. degrees in Electrical and Computer Engineering from the California State Polytechnic University in Pomona with an emphasis in digital signal processing and filter design. Steve joined JPL in 1994 and the PSDG group in 2001, where he has worked as a signal analysis engineer for open loop receivers and antenna arraying systems. Steve has recently been the task manager for several projects including the Wideband VLBI Science Receiver (WVSR), the Deep Space Communications Complex (DSCC) VLBI processor (DVP), and the DSCC downlink Array (DDA).*

***Robert Navarro*** *received a B.S in Engineering from Harvey Mudd College in 1986 and a M.S. in Electrical Engineering in 1987. He has been with JPL for more than 21 years. He has worked on DSN ground systems for radio science and VLBI recording as well as correlators and antenna arrays as an engineer and a manager. He is currently Deputy Manager of the Telemetry, Tracking and Command End-to-End Data Office for the Deep Space Network Project. His career started with Hewlett Packard working on circuit design and image processing for ink jet printers.*

***Douglas Wang*** *is a senior hardware design engineer. He developed many electronic components for flight control computers, autonomous landing guidance, millimeter wave radar, cell phone GPS receiver, and the MSL rover power analog module. He has a BSEE from Cal Poly Pomona and a master's degree from USC. Doug is the DDA Hardware Cognizant Engineer.*